EVALUATION OF THE SAFE OPERATING AREA OF A 2.0 CM^2, 4 KV SI SGTO

H. O'Brien, W. Shaheen*, T. Crowley*, S.B. Bayne
U.S. Army Research Laboratory, 2800 Powder Mill Road
Adelphi, MD 20783 USA

Abstract

The U. S. Army Research Laboratory (ARL) has been evaluating high voltage, high current modular silicon Super-gate turn-off thyristors (SGTOs) developed by Silicon Power Corporation (SPCO) for ARL. SGTOs were characterized at the individual chip level in order to help understand the capabilities of any scaled up device packages. SGTOs were individually pulsed in two separate test beds: one designed to produce narrow current pulses, and another designed for wider pulses reaching 1 ms. Peak current, rise time and action (I^2t) limitations were evaluated across this spectrum of pulse widths to document the Safe Operating Area (SOA) of the Si SGTOs. The peak current attained at a 1.9 µs FWHM pulse width was 20 kA with a 10-90% rate-of-current rise of 26 kA/µs. In the wider pulse circuit, single die were switched as high as 6.2 kA with an action value of 18 x 10^3 A^2s. Waveforms for various SGTOs were analyzed, and a set of SOA curves was created to represent characterization of the SGTO die. An exploration to minimize recovery time (Tq) is also included, with Tq time reduced to 10 µs following a 1-ms wide, 5 kA pulse.

I. INTRODUCTION

Army survivability and lethality applications require compact, high power switches that can deliver current at a range of different pulse widths, amplitudes and rise times. The modular approach, combining SGTO die in parallel and in series, has been successful for devices implemented in both 10 kV, 80 kA and 10 kV, 400 kA configurations [1]. ARL is conducting a more thorough exploration of the capabilities of SPCO's SGTO die in order to determine what advantages it may have over full wafer-scale thyristors (125-150 mm diameter). Key parameters being studied are peak current, dI/dt, action and Tq.

The SGTO (also known as the current controlled Solidtron, or CCS) is rated for 4 kV forward blocking and 10 kA pulse current at 10 µs pulse widths, or 100 A continuous [2]. Many devices were high-potted beyond 4 kV while showing less than 100 µA of current leakage. Each chip has a footprint of 3.5 cm^2 and an active (cathode mesa) area of 2.0 cm^2. Recommended gate current for turn-on is 0.5-1 A applied relative to the cathode. A cell-based emitter design and integrated gate and cathode fingers are intended to aid in rapid turn-on and even current distribution.

To supply this study, partially failed SPCO modules containing eight Si die were altered so that each device could be switched independently while the other seven remained unused. Figures 1 and 2 show a single SGTO die and the interior of an 8-die module. Gate, cathode and edge terminations are on the top side of the chip, while the underside serves as an anode connection point.

Figure 1. A single Si Super-GTO, cathode side up. Footprint: 2.3 cm long by 1.5 cm wide.

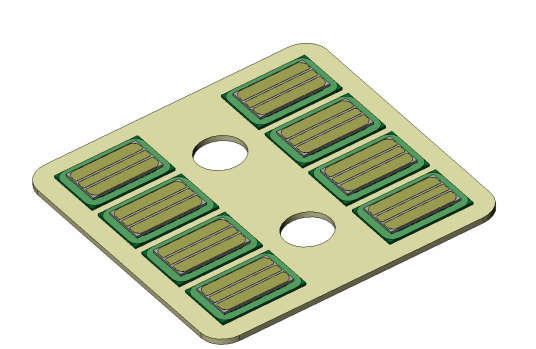


Figure 2. Eight-SGTO layout with a single anode base plate, 8.0 cm per side.

The following sections include procedures and resulting data for SGTOs pulsed in two different test beds: one low inductance, low resistance circuit producing high current at a narrow pulse width, and one large inductance, large capacitance circuit producing wider, half-sine shaped pulses.

* *Berkeley Research Associates, 6551 Mid Cities Avenue, Beltsville, MD 20705 USA*

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
JUN 2007	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Evaluation Of The Safe Operating Area Of A 2.0 Cm2, 4 Kv Si Sgto	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **U.S. Army Research Laboratory, 2800 Powder Mill Road Adelphi, MD 20783 USA**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002371. 2013 IEEE Pulsed Power Conference, Digest of Technical Papers 1976-2013, and Abstracts of the 2013 IEEE International Conference on Plasma Science. IEEE International Pulsed Power Conference (19th). Held in San Francisco, CA on 16-21 June 2013., The original document contains color images.

14. ABSTRACT
The U. S. Army Research Laboratory (ARL) has been evaluating high voltage, high current modular silicon Super-gate turn-off thyristors (SGTOs) developed by Silicon Power Corporation (SPCO) for ARL. SGTOs were characterized at the individual chip level in order to help understand the capabilities of any scaled up device packages. SGTOs were individually pulsed in two separate test beds: one designed to produce narrow current pulses, and another designed for wider pulses reaching 1 ms. Peak current, rise time and action (I2t) limitations were evaluated across this spectrum of pulse widths to document the Safe Operating Area (SOA) of the Si SGTOs. The peak current attained at a 1.9 ìs FWHM pulse width was 20 kA with a 10-90% rate-ofcurrent rise of 26 kA/ìs. In the wider pulse circuit, single die were switched as high as 6.2 kA with an action value of 18 x 103 A2s. Waveforms for various SGTOs were analyzed, and a set of SOA curves was created to represent characterization of the SGTO die. An exploration to minimize recovery time (Tq) is also included, with Tq time reduced to 10 ìs following a 1- ms wide, 5 kA pulse.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**SAR**	**6**	

II. NARROW PULSE

A. Procedure

The lower-energy test bed utilized for narrow pulse switching was designed to produce up to 20 kA of current from a 5 kV initial charge. Voltage was limited by the ratings of both the SGTOs and the pulse capacitors used. It was hypothesized that the devices would be able to perform beyond 10 kA at very narrow pulse widths. The general procedure for each test shot involved charging up a small capacitor bank to a chosen voltage level and then triggering the SGTO on to dump the energy through a resistive load. Inductance between capacitors and leading to and from the switch was kept to a minimum in order to maximize output current and dI/dt. Low loop inductance on the order of 100 nH was also key to keeping the FWHM pulse width to 2 µs. Part of the motivation for using this pulse width was to allow for fairly direct comparison between the Si SGTO and previously evaluated SiC thyristors [3]. A schematic of the pulse circuit is shown in Figure 3, followed by a photo of the actual circuit in Figure 4.

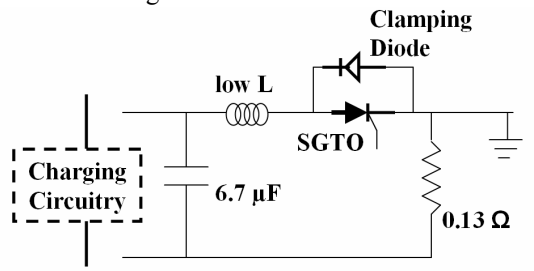


Figure 3. Schematic of circuit used for narrow pulse evaluations. The complete loop inductance is estimated to be 100 nH. The anti-parallel clamping diode conducts reversal current so that negative current does not flow through the SGTO.

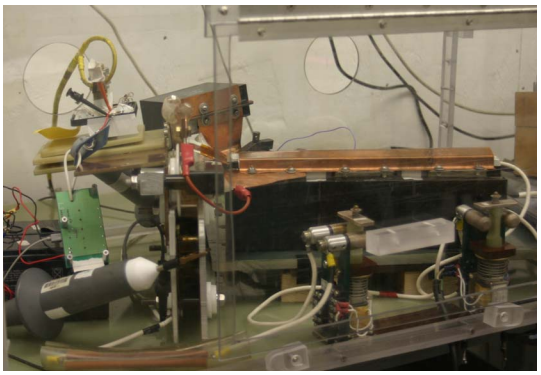


Figure 4. Photo of the test bed. Copper strips were used to connect capacitors to each other and to the device under testing. Aluminum plates clamped the resistive load. Safety relays can be seen to the right. The whole test bed was covered by a Lexan box.

Multiple devices were pulsed at a widely spaced single-shot rate at increasing voltage and current up to the point of failure. Another SGTO was pulsed in 1-Hz bursts of 1000 shots each at current levels ranging 10 kA – 15 kA. One other device was similarly switched but at a 5-Hz rate up to 17 kA. For both 1-Hz and 5-Hz switching, an IGBT was added between the charging circuitry and the capacitor bank to provide fast disconnect prior to SGTO pulses and fast reconnect after each pulse. Because the SGTO did not turn off immediately when the pulse current dropped to zero, it would continue to conduct as long as the power supply was connected. This would cause the over-current safety on the power supply to trip. Adding the IGBT and triggering it in synch with the SGTO gate trigger solved this problem.

B. Results

The peak current attained at the narrow pulse width was 20 kA. With the first SGTO, this shot was repeated twice before apparent failure at the gate-cathode junction. With the second SGTO, this shot was only completed once before gate failure was noticed. The full 5 kV was still held off at the anode. Figure 5 shows the recorded voltage and current waveforms for a typical 20 kA pulse.

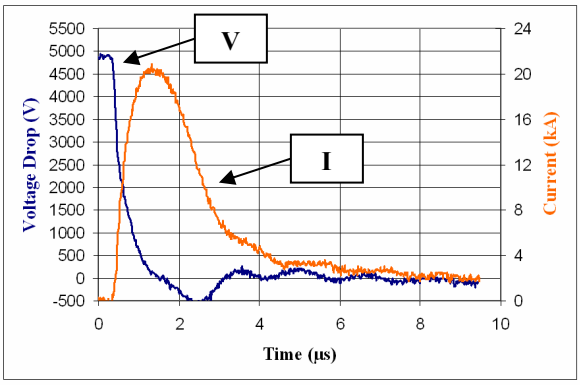


Figure 5. Waveforms for peak single-shot current pulse. Anode-cathode voltage drop was measured at the switch buss and likely includes some small inductance. Peak current was 20 kA.

The pulse width of the current waveform was 1.9 µs at 50% of peak current and about 10 µs across the full base width. The peak current density was 10 kA/cm^2 over the active (mesa) area of the device. The resulting action, or I^2t, was calculated to be 680 A^{2}s. The rate of current rise was 26 kA/µs as measured across the 10-90% portion of the current rise. This was the peak dI/dt reached, partially limited by the amount of system inductance. SPCO lists the devices' maximum dI/dt as 30 kA/µs. [2]

Because the SGTO module is encapsulated with a hard epoxy, devices could not simply be examined under the microscope for points of failure. One hypothesis is that concentrated heating from the fast, high current pulse damaged the passivation at the interface of the gate and cathode fingers. Because the devices evaluated at the single-shot rate could still block high voltage but could not be biased on, it seemed unlikely that the high current

or physical pulse stresses had cracked through the layers of the devices.

For repetitive switching, the devices were pulsed at a lower voltage and current. The device pulsed at 1 Hz was switched 1000 times at each of five peak current levels before failure: 11 kA, 12 kA, 13 kA, 14 kA and 15 kA. The SGTO sped up to 5 Hz was also pulsed 1000 times each at the current levels listed above, as well as up to 16 kA and 17 kA. At any current level, there was no notable difference in performance between the first test shot and the 1000th shot. Overlapping current waveforms for 17 kA, 5 Hz switching are shown in Figure 6.

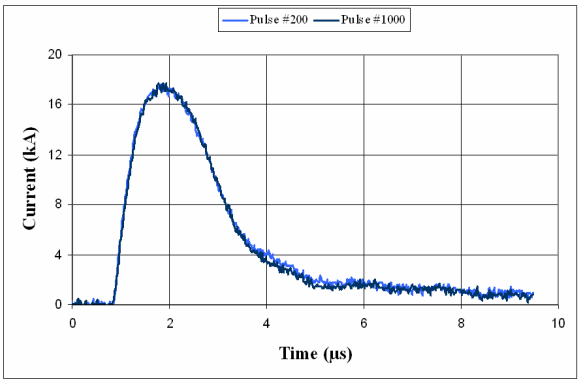


Figure 6. Pulse #200 and pulse #1000 for 5-Hz switching at a current peak of 17 kA. Applied voltage was 4.5 kV. Rate of current rise was 23 kA/µs.

The repetitively switched SGTOs did not show the gate damage seen in the devices that were pulsed at a single-shot rate. This may be due to the lower peak current levels, suggesting that over-currenting is more damaging to the SGTOs than repetitive switching. It is worth noting again that all of the SGTOs involved in this study were previously stressed in some way as part of a full module.

III. WIDE PULSE

A. Procedure

Present Army applications call for switches that can perform at pulse widths exceeding 1 ms and have relatively fast recovery. A simulation was run in order to determine an appropriate amount of capacitance, inductance and resistance to produce a current waveform that was 1 ms across the base, had the shape of a half-sine curve and peaked at 4-6 kA within the voltage limitations of the SGTOs. The resulting circuit is shown in Figure 7. A photo of the test bed is in Figure 8. The inductors shown were designed and mounted in-house.

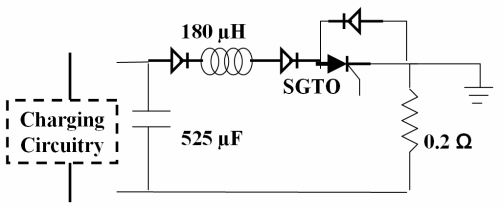


Figure 7. Schematic of wide pulse circuit. Larger inductance and capacitance created an under-damped system for a wide pulse with slow rise time. Diodes clamped ringing caused by the inductor.

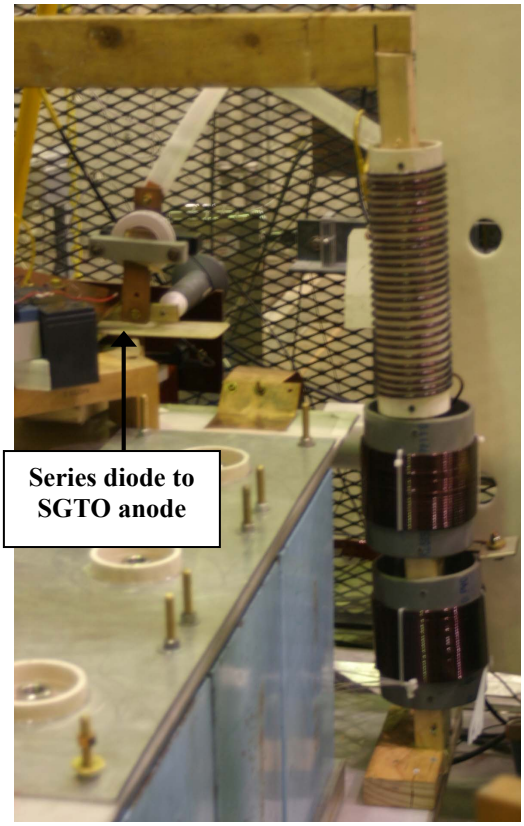


Figure 8. Wide pulse test bed. To shape the output current pulse, inductance between capacitors was kept low with parallel plates. Series inductors totaling 180 µH fed current to the switch.

In all of the high power SGTO test beds, a diode is connected in anti-parallel with the device under testing in order to clamp negative current and protect the switch in case of a failure anywhere in the system. For the wide pulse test bed, diodes were also added in series with the inductor to limit the ringing at the capacitor. Without these diodes, the switch would end up pulsing positive more than once per test shot.

Several SGTOs were pulsed at increasing voltage and current with ample spacing between switching events. Once a safe, repeatable peak current was settled on, it was of interest to determine the recovery time of the SGTO

given that amount of stress and heating. The parameter studied was Tq, or the amount of down time between when the main current returns to zero and when high voltage can be reapplied at the anode with confidence that the device will have returned to blocking mode.

Tq was mostly evaluated with an applied (and re-applied) voltage of 4 kV and a 1-ms current pulse of 5 kA. Initially, many mill-seconds were allowed to pass after the end of the current pulse before re-applying high voltage. With each successive test shot, this delay time was shortened so long as the SGTO had successfully completed turn-off. For the test setup, a second smaller capacitor bank of about 6 µF was used to store the added energy. An IGBT was triggered to rapidly apply the voltage at a given delay time, with the dV/dt shaped by a series resistor and small parallel capacitor. SPCO provides a rating for rate of change of voltage immunity, but it only applies to the off-state, single-shot case when a 10 ohm resistor is connected to short the gate to the cathode [2]. The experiments described in this paper mostly took place with the SGTO not fully turned off and the 10 ohm gate-cathode resistor removed, so the shape and slope of the dV/dt affected the recovery differently. A general block diagram of the test setup is shown in Figure 9.

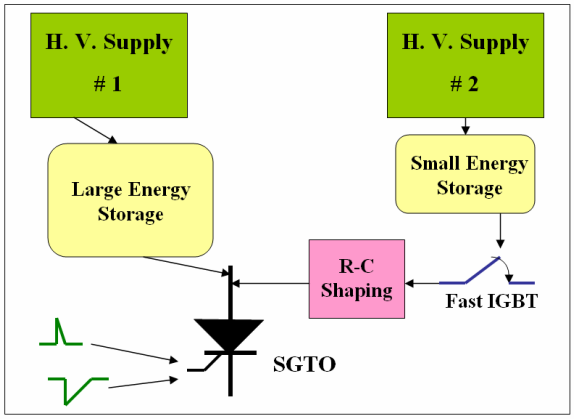


Figure 9. General block diagram of the circuitry involved in the Tq evaluation. The positive gate pulse was for turn-on; the negative gate pulse aided turn-off and will be discussed in the Results section.

An additional diode was added where the R-C shaping components fed into the anode of the SGTO. The diode which was already in place between the inductor and the SGTO's anode (refer back to Figure 7) ensured that during the secondary high voltage application, the inductor and main energy storage bank were not drawing current.

B. Results

SGTOs pulsed at increasing current to failure reached a peak current of 6.2 kA. Across the range of devices evaluated, this was not considered a very reliable, repeatable current, so 5 kA was settled on as a safe current for wide pulses. With some devices, once 5 kA was exceeded, a brief increase in voltage drop would appear more than halfway through the current pulse. If the device was repeatedly pulsed at that current level, it would fail after a couple of shots. The timing of this voltage change suggests that it is due to the build-up of heat over the course of the current pulse. Heating may have affected the resistance of the solder joints within the package, or it could have damaged sections of the silicon, affecting the voltage drop. A repeatable 5 kA test shot is shown in Figure 10, followed by a higher test shot with signs of failure in Figure 11. When SGTOs did fail due to current and heating, they typically were shorted anode-to-cathode.

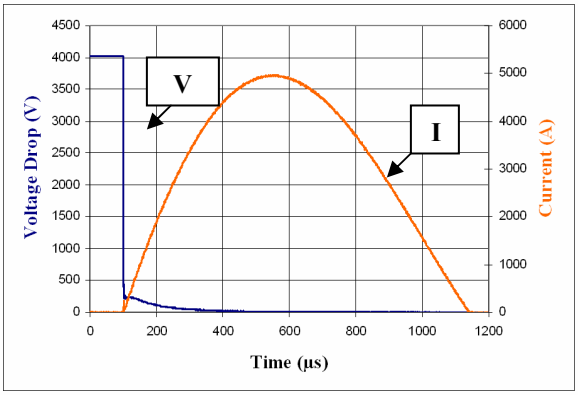


Figure 10. Voltage and current waveforms for 5 kA, 1 ms pulse.

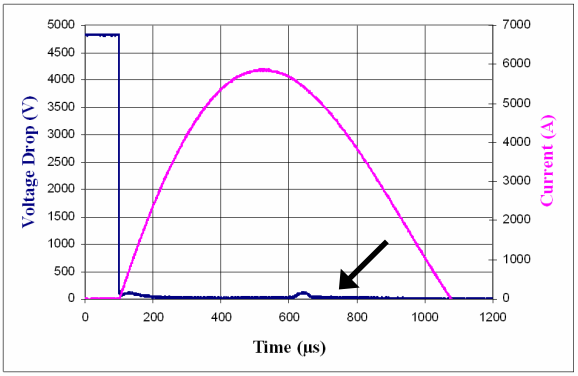


Figure 11. Voltage and current waveforms for 5.8 kA, 1 ms pulse. Note brief increase in voltage drop just beyond the time of peak current.

For the 5 kA pulse, the calculated action was 13000 A^2s, almost twenty times the action of the peak narrow pulse. The current density was 2.5 kA/cm^2.

The first round of Tq evaluation found that the SGTO was not fully off for milliseconds after the end of the current pulse. High voltage was re-applied, but without pulling the gate negative, the remaining minority carriers within the device allowed it to turn back on even without an applied trigger, as shown in Figure 12. Increasing the charge resistor to slow the dV/dt application was not

effective enough. It was determined that gate-assisted turn-off would be a good solution for reducing the Tq to the ten's of microseconds time frame.

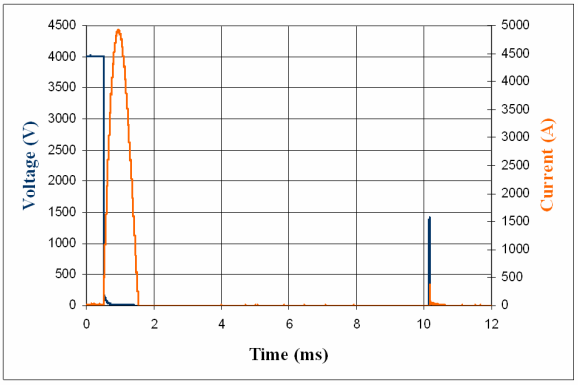


Figure 12. Long Tq. Note ms time scale. This device started to block when high voltage was re-applied at the 10-ms mark, but reverted back into the on-state.

Gate-assisted turn-off was achieved by changing the gate driver board. The original board in use, from SPCO, was optimized for turn-on of the SGTO. A new board was designed that incorporated both an IGBT triggering method and a separate negative gate pulse with a delay time adjustable at the pulse generator. The main driver's voltage output was held to -10 V except during the 10 µs it was triggered positive to turn on the SGTO. Adding this negative voltage bias decreased the Tq by a few milliseconds, but even shorter delay time was desired. This portion of the driver was retained but an extra negative pulse of current was added, positioned to be delivered when the main anode current reached zero. Applying -5 A of current brought the Tq under 100 µs. Applying -29 A of current reduced the Tq all the way to 30 µs. The negative gate current waveform is shown in Figure 13, with the overall current pulse and high voltage blocking shown in Figure 14. The Tq study is ongoing, with the goal of optimizing the driver and determining the trade-offs between what Tq is desired for an application and what volume and power requirements the driver needs to produce that given recovery time. Adjustments are also being made to the shape of the negative current pulse and the dV/dt rate of the high voltage at the anode.

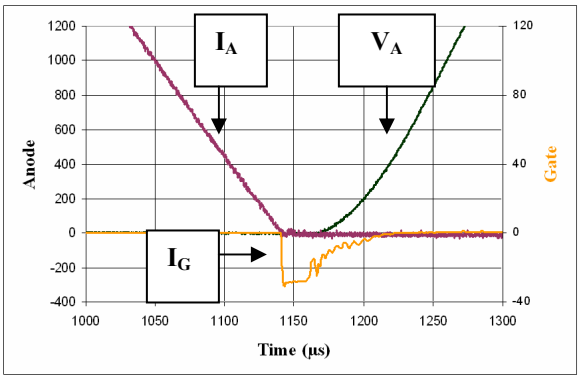


Figure 13. Tq of 30 µs with -29 A applied at the gate (I_G).

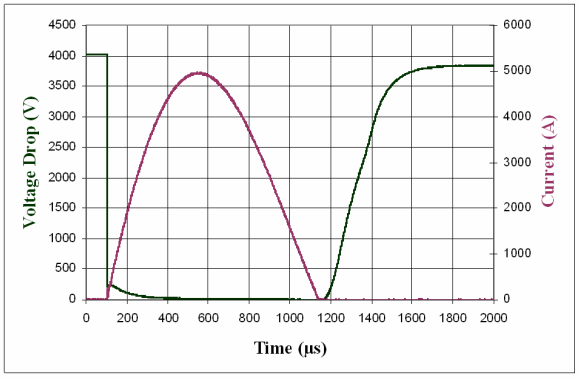
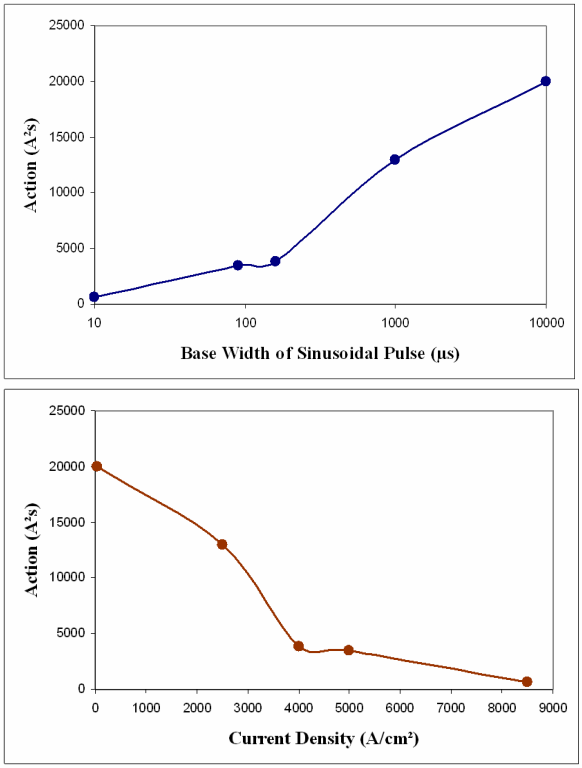


Figure 14. 4 kV applied, 5 kA pulsed and 4 kV reapplied and fully blocked after 30 µs.

IV. SUMMARY

Silicon Super-GTOs were switched at both narrow and wide currents to increase understanding of their range of capabilities and applications. At a 1.9 µs FWHM pulse width, a dI/dt of 26 kA/µs was reached, and devices were switched over 1000 times at 17 kA peak current. At a 1 ms base pulse width, SGTOs were switched several times at 5 kA and 13000 A^2s without failure. Action (I^2t) values were much higher at the wider pulse width. A preliminary Safe Operating Area profile can be put together like the ones in Figures 15 and 16.



Figures 15 & 16. Preliminary SOA profiles for Si SGTO with (logarithmic) pulse width vs. action and current density vs. action.

Gate-assisted turn-off was revealed as the optimum way to minimize recovery time following a 1-ms wide pulse. The gate drive requirements are still being evaluated, but with a fast-falling input of -29 A timed at the end of the 5 kA main pulse, Tq was reduced to 30 μs. After settling on a driver for the single SGTO chip, a full 8-chip module will be evaluated to determine if its wide pulse switching capabilities and gate turn-off requirements scale up from those of the single SGTO.

V. REFERENCES

[1] H. O'Brien, W. Shaheen, R.L. Thomas, Jr., T. Crowley, S.B. Bayne, and C. J. Scozzie, "Evaluation of Advanced Si and SiC Switching Components for Army Pulsed Power Applications," *IEEE Trans. Magn.*, vol. 43, no. 1, pp. 259-264, Jan. 2007.

[2] K. Brandmier, "Solidtron™ CCSTA14N40 N-Type, ThinPak™ Preliminary Data Sheet," Silicon Power Corp., Malvern, PA, 2005.

[3] H. O'Brien, W. Shaheen, S. B. Bayne, "Pulsed Power Switching of a 4 mm x 4 mm SiC Thyristor," 15th IEEE Intl. Pulsed Power Conference, Monterey, CA, June 2005.